

REMARKS**I. Status of the Application**

Claims 15, 16, 19-22, 25, 26, 28 and 34-38 are pending in this application. In the July 12, 2007 office action, the Examiner:

- A. Rejected claims 15-16, 19-22, 25, 26, 28 and 34-38 under 35 U.S.C. §112, second paragraph, for allegedly failing to point out subject matter regarded as the invention;
- B. Rejected claims 15, 19-22, 25, 26 and 34-38 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,573,776 to Miyamoto (hereinafter "Miyamoto"); and
- C. Rejected claims 16, 28 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Miyamoto in view of U.S. Patent No. 6,208,183 to Li et al. (hereinafter "Li").

In this response, applicants have amended claims 15 and 22 to further clarify the claimed subject matter. Applicants respectfully traverse the rejections of the pending claims and request reconsideration of the application in view of the foregoing amendments and accompanying remarks.

II. The Indefiniteness Rejection Should be Withdrawn

The Examiner rejected claims 15-16, 19-22, 25, 26, 28 and 34-38 as allegedly being indefinite. The rejection was based solely on a limitation found only in independent claims 15 and 22. (July 12, 2007 office action at p.2). In particular, the Examiner stated that the limitation "a second delay time is set in the second delay element as a function of the frequency of the first input" was not clearly understood because figure 2 of the application does not show "any kind of feedback to control 'the second delay element'. (July 13, 2007

office action at p.2).

It is respectfully submitted that the phrase is sufficiently clear when read in context in the claim. For example, the entire relevant context from claim 15 is set forth below:

wherein the delay device further comprises a *frequency detection unit having an output signal* used to adjust the at least one second delay element such that a second delay time is set in the second delay element as a function of the frequency of the first input...

(emphasis added)

Thus, claim 15 actually recites that a *frequency detection unit* has an output signal that is used to adjust the second delay element such that a second delay time is set as a function of the frequency of the first input. An exemplary embodiment of this is clearly shown in the drawings. For example, Fig. 2 as filed shows a frequency detection unit 110 that detects the frequency of a signal at the first input 103 and is used to adjust the second delay element 102.

One of ordinary skill in the art would readily identify that a frequency detection unit may have an output signal that is used to adjust another device based on a first input signal.

Nevertheless, applicants have further clarified the claim language in both claims 15 and 22 to recite that the frequency detection unit actually *detects* the frequency of the first input unit, in addition to having the claimed output signal.

In view of the foregoing amendments and arguments, it is respectfully submitted that claims 15 and 22 are *not* indefinite. Because independent claims 15 and 22 are not indefinite, it is respectfully submitted that claims 16, 19-21, 25, 26, 28 and 34-38 are not indefinite. As a consequence, the indefiniteness rejections of claims 15, 16, 19-22, 25, 26, 28 and 34-38 should be withdrawn.

III. The Anticipation Rejection of Claim 15

Claim 15 stands rejected as allegedly being anticipated by Miyamoto. As will be discussed below in detail, Miyamoto fails to disclose each and every element of claim 15.

A. The Invention of Claim 15

Claim 15 is directed to a delay lock loop apparatus which can be adapted for use with a broad range of externally generated clock signals. The apparatus includes a delay device, a feedback device, a frequency detection device and a phase difference detection device. The delay device comprises first and second delay elements. The second delay element comprises *different second delay elements* providing different delay times for the second delay element *for different frequency ranges*. At least one second delay element is for low frequency ranges of the clock signal, and at least one further second delay element is for high frequency ranges of the clock signal. Thus, claim 15 requires that the second delay includes different delay elements providing different delay times for different frequency ranges.

B. Miyamoto Fails to Disclose Different Delay Elements for High and Low Frequencies.

Miyamoto fails to disclose, among other things, a “second delay element [comprising] different second delay elements in discrete steps providing different delay times for the second delay element for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal”, as claimed in claim 15. In general, Miyamoto uses a single delay unit (e.g. delay line 23) carried out as

a single line of delay elements. The single delay unit 23 provides a variable delay by causing output of the delayed signal from different ones of the delay elements. (Miyamoto at col. 8, line 62 to col. 9, line 24).

Hence, Miyamoto does not disclose *different delay elements* for different frequency ranges. Instead, the same elements are used for all frequency ranges, even though the number that are used may be less for higher frequencies. Thus, for example, there is no delay element that is used for high frequency ranges that is *not also* used for low frequency ranges. To the extent some of the delays 23-0 through 23-7 are used for high frequencies, that same group of delays is also used for low frequencies.

C. The Examiner's Rejection

The Examiner has identified the delay line 22 as being the second delay element of claim 15. Applicants disagree. The delay line 22 does not actually generate a delayed clock signal A, but rather controls the delay line 23. The delay line 23 delays the clock signal A. Regardless, the delay line 22 is identical to the delay line 23 in the respect that both high and low frequency signals use the same single delay element line.

D. Conclusion as to Claim 15

Because Miyamoto fails to disclose a “second delay element [comprising] different second delay elements in discrete steps providing different delay times for the second delay element for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal”, as claimed in

claim 15, it is respectfully submitted that the rejection of claim 15 over Miyamoto is in error and should be withdrawn.

IV. Claims 19-21 and 34-38

Claims 19-21 and 34-38 all stand rejected as allegedly being anticipated by Miyamoto. Claims 19-21 and 34-38 all depend from and incorporate all of the limitations of claim 15. Accordingly, for at least the same reasons as those set forth above in connection with claim 15, it is respectfully submitted that the anticipation rejection of claims 19-21 and 34-38 is in error and should be withdrawn.

V. Claims 16 and 35

Claims 16 and 35 stand rejected as allegedly being obvious over Miyamoto in view of Li. Claims 16 and 35 both depend from and incorporate all of the limitations of claim 15. Accordingly, each of claims 16 and 35 incorporates a limitation directed to a “second delay element [comprising] different second delay elements in discrete steps providing different delay times for the second delay element for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal”. As discussed above in connection with claim 15, Miyamoto fails to teach or suggest such a second delay element.

The Examiner cites Li as providing the teaching of using a filter to remove interfering signals. (July 13, 2007 office action at p.5). Accordingly, the modification of Miyamoto proposed by the Examiner in the rejection of either of claims 16 or 35 does not cure the

deficiency of Miyamoto with respect to claim 15. Accordingly, for at least the same reasons as those set forth above in connection with claim 15, it is respectfully submitted that the obviousness rejections of claim 16 and 35 are in error and should be withdrawn.

VI. The Rejection of Claim 22 is in Error

Claim 22 also stands rejected as allegedly being anticipated by Miyamoto. Claim 22 is directed to a method of providing clock signals to a circuit that includes a step of:

delaying the external clock signal with the at least one frequency variable delay element and providing the delayed external clock signal to the first variable delay element, wherein the frequency variable delay element comprises different second delay elements in discrete steps providing different delay times for the second delay element for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal

As discussed above, Miyamoto does not teach “different second delay elements in discrete steps providing different delay times for the second delay element for different frequency ranges, at least one second delay element being for low frequencies of the externally generated clock signal and at least one further second delay element being for high frequencies of the externally generated clock signal”.

Because Miyamoto does not teach the different second delay elements as claimed, it is respectfully submitted that the rejection of claim 22 over Miyamoto is in error and should be withdrawn.

VII. Claims 25, 26 and 28

Claims 25, 26 and 28 all stand rejected as allegedly being anticipated by Miyamoto. Claims 25, 26 and 28 all depend from and incorporate all of the limitations of claim 22.

Accordingly, for at least the same reasons as those set forth above in connection with claim 22, it is respectfully submitted that the anticipation rejection of claims 25, 26 and 28 is in error and should be withdrawn.

VIII. Claim 28

Claims 28 stands rejected as allegedly being obvious over Miyamoto in view of Li. Claims 28 depends from and incorporates all of the limitations of claim 22. As discussed above in connection with claim 22, Miyamoto fails to teach or suggest different second delay elements as recited in claim 22. The modification of Miyamoto proposed by the Examiner in the rejection of claim 28 does not cure the deficiency of Miyamoto with respect to claim 22. Accordingly, for at least the same reasons as those set forth above in connection with claim 22, it is respectfully submitted that the obviousness rejection of claim 28 is in error and should be withdrawn.

IX. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is therefore respectfully requested.

In the event applicant has inadvertently overlooked the need for an extension of time or payment of an additional fee, the applicant conditionally petitions therefore, and authorizes any fee deficiency to be charged to deposit account 13-0014.

November 13, 2007

Respectfully submitted,


Harold C. Moore
Attorney for Applicants
Attorney Registration No. 37,892
Maginot Moore & Beck
Chase Tower
111 Monument Circle, Suite 3250
Indianapolis, Indiana 46204-5109
Telephone: (317) 638-2922